In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1. (Currently Amended) An apparatus comprising:

a memory;

a plurality of processors coupled to ~~a controller and a~~ the memory; and

a [[the]] controller coupled to the memory and the plurality of processors, the controller to execute a debug process~~, said debug process~~ that:

attaches at least one breakpoint bit field directly to ~~each~~ one or more instructions of [[a]] the plurality of processor ~~instructions~~, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of the particular instruction without having to perform an address comparison;

manipulates ~~wherein said controller adds~~ at least three debug register bit fields [[to]] of at least one processor control status register ~~field~~, ~~wherein said~~ the at least three register bit fields comprise a run field, a single step field, and a debug enable field; and

accesses an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM instruction (LDTI) and a Load from Instruction RAM (LDFI) instruction.

2. (Currently Amended) The apparatus of claim 1, wherein said at least one breakpoint bit field allows a breakpoint to be one of set and not set for each of said

~~plurality of~~ one or more instructions.

3. (Cancelled)

4. (Cancelled)

5. (Previously Presented) The apparatus of claim 1, wherein said single step field allows a set of instructions to each be single-stepped through one cycle at a time.

6. (Previously Presented) The apparatus of claim 1, wherein said debug enable field one of enables and disables a debug mode.

7. (Currently Amended) The apparatus of claim 1, wherein ~~at least one instruction~~ the LDTI instruction loads content of ~~at least one~~ a register a processor of the plurality of processors into an instruction memory coupled to ~~said at least one~~ the processor ~~of the plurality of processors~~ via a bus.

8. (Currently Amended) The apparatus of claim 7, wherein the LDFI instruction loads the content of ~~said~~ the instruction memory ~~is loaded~~ into [[a]] the register coupled to ~~said at least one~~ the processor ~~of the plurality of processors~~.

9. (Cancelled)

10. (Withdrawn) A system comprising: a plurality of image signal processors (ISPs), each ISP including a plurality of processor elements (PEs), the plurality of ISPs including: a debug instruction register coupled to a first mux element, an instruction memory coupled to an instruction register, a decoder coupled to said instruction register, an execution unit coupled to said decoder, a debug executive unit coupled to said instruction memory, and a second mux element coupled to said execution unit and a plurality of local registers, wherein the decoder to decode at least one breakpoint bit field of each of a plurality of instructions.

11. (Withdrawn) The system of claim 10, wherein said plurality of ISPs arranged in a matrix pattern and each having quad-ports.

12. (Withdrawn) The system of claim 11, said plurality of PEs each coupled to a register file switch.

13. (Withdrawn) The system of claim 10, the decoder to decode at least three debug register bit fields of a control status register, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

14. (Withdrawn) The system of claim 13, said single step field allows a set of instructions to each be single stepped through one instruction at a time.

15. (Withdrawn) The system of claim 10, wherein at least one instruction loads

content of said debug instruction register into said instruction memory.

16. (Withdrawn) The system of claim 15, wherein content of said instruction memory is loaded into said debug instruction register.

17. (Withdrawn) The system of claim 16, wherein internal states of said plurality of PEs are accessible through said debug instruction register.

18. (Currently Amended) An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

adding at least one breakpoint bit field directly to each of a plurality of instructions to execute on a plurality of processors, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of the particular instruction without having to perform an address comparison;

manipulating ~~adding~~ at least three debug register bit fields ~~directly to~~ of at least one processor control status register ~~field said~~, the at least three register bit fields comprise a run field, a single step field, and a debug enable field; and

accessing an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM instruction (LDTI) and a Load from Instruction RAM (LDFI) instruction.

19. (Previously Presented) The apparatus of claim 18, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of said breakpoint bit, and

setting a breakpoint for an instruction if it is determined that said state of said at least one breakpoint bit field is set.

20. (Cancelled)

21. (Currently Amended) The apparatus of claim 19 [[20]], further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a run field bit, ~~and~~

running a set of instructions if said state of said run field bit is set, and

stopping a set of instructions if said state of said run field bit is not set.

22. (Currently Amended) The apparatus of claim 21, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a single step bit, and

single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

23. (Currently Amended) The apparatus of claim 18, wherein ~~further containing~~.

~~instructions which, when executed by a machine, cause the machine to perform operations including:~~ the LDTI instruction loads[[ing]] content of at least one register into an instruction memory, and wherein the LDFI instruction loads[[ing]] content of said instruction memory into the at least one register~~, and~~

~~accessing internal states of each of a plurality of processors through a debug process.~~

24. (Currently Amended) A method comprising:

adding at least one breakpoint bit field directly to each of a plurality of instructions to execute on a plurality of processors, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of the particular instruction without having to perform an address comparison;

manipulating ~~adding~~ at least three breakpoint register bit fields [[to]] of at least one processor control status register ~~field~~, the at least three register bit fields comprise a run field, a single step field, and a debug enable field; and;

accessing an internal status of one or more of the plurality of processors by utilizing at least one of a Load to Instruction RAM instruction (LDTI) and a Load from Instruction RAM (LDFI) instruction;

wherein the ~~attached~~ at least one breakpoint bit field is an additional field directly added to each processor instruction.

25. (Currently Amended) The method of claim 24, further comprising:

determining a state of a breakpoint bit, and

setting a breakpoint for an instruction if it is determined that said state of said breakpoint bit is set.

26. (Original) The method of claim 24, further comprising:

running a debug process on a host device, and

entering debug commands through a graphical user interface.

27. (Cancelled)

28. (Currently Amended) The method of claim 24, further comprising:

determining a state of a single-step bit, and

entering commands for single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

29. (Currently Amended) The method of claim 24, ~~further comprising:~~ wherein the LDTI instruction loads[[ing]] content of at least one register into an instruction memory, and wherein the LDFI instruction loads[[ing]] content of said instruction memory into the at least one register~~, and accessing internal states of each of a plurality of processors through said debug process, wherein accessing includes reading state values and overwriting state values~~.